**IN THE CLAIMS:**

Please cancel claims 28-30 and 38-40 without prejudice.

1. (Original) A method for pre-decoding instructions prior to storage of the instruction in a level one cache for a processor core, for managing power dissipation in the processor core, the method comprising:

re-encoding an opcode of an instruction to incorporate a power token, the power token comprising a bit to indicate a unit of the processor core to turn off during execution of the instruction; and

adjusting the power dissipation in the processor core based upon a state of management control bits associated with the power dissipation, in response to a dynamic power count for the processor core based upon issuance of the instruction.

2. (Original) The method of claim 1, further comprising adjusting the frequency of the processor core and the voltage of the processor core in response to the dynamic power count.

3. (Original) The method of claim 1, further comprising adjusting the power dissipation in the processor core based upon a threshold associated with the dynamic power count, the threshold being related to a physical limitation of the processor core.

4. (Original) The method of claim 1, further comprising modifying execution flags associated with the instruction, the execution flags to schedule issuance of the instruction with respect to other instructions in a parallel execution group that comprises the instruction.

5. (Original) The method of claim 1, wherein re-encoding the opcode comprises selecting the power token from a look-up table, wherein the look-up table comprises the

power token and other power tokens for instructions to be executed by the processor core.

6. (Original) The method of claim 1, wherein re-encoding the opcode comprises selecting the a new opcode that identifies the instruction and power dissipation associated with the instruction.

7. (Original) The method of claim 6, wherein the opcode and the new opcode utilize an equal number of bits.

8. (Original) A method, comprising:

monitoring an instruction execution rate for a processor core;

creating a dynamic power count representative of power dissipation in the processor core based upon the instruction execution rate; and

pre-decoding instructions prior to storage in a level one cache to dynamically adjust power dissipation by the processor core based upon the dynamic power count.

9. (Original) The method of claim 6, wherein pre-decoding comprises:

generating a power token for an instruction of the instructions, wherein the power token is associated with a relative average power that the instruction consumes during execution; and

re-encoding an opcode of the instruction to include the power token.

10. (Original) The method of claim 9, wherein re-encoding an opcode comprises ranking the instructions based upon power dissipated by each of the instructions and encoding the opcode based upon the ranking.

11. (Original) The method of claim 9, wherein monitoring comprises selecting valid completions associated with the instructions.

12. (Original) The method of claim 11, wherein creating the dynamic power count comprises summing the power token with other power tokens associated with the valid completions and adding the sum of the power tokens to a total dynamic weighted execution rate.

13. (Original) The method of claim 12, wherein creating the dynamic power count comprises periodically loading the total dynamic weighted execution rate into a buffer.

14. (Original) The method of claim 8, wherein pre-decoding comprises identifying a set of the instructions, each instruction of the set having a result that is independent of the results of other instructions in the set.

15. (Original) The method of claim 8, wherein pre-decoding comprises delineating a group of the instructions for parallel execution based upon stop bit execution flags associated with the instructions.

16. (Original) The method of claim 15, wherein pre-decoding comprises selecting instructions from the group to modify the dynamic power count, based upon a state of management control bits, to determine a parallel instruction issue schedule.

17. (Original) The method of claim 16, wherein selecting instructions from the group comprises adjusting execution flags associated with the instructions to decrease the dynamic power count.

18. (Original) The method of claim 8, wherein pre-decoding comprises incorporating a bit in a power token associated with the instructions to control clock degating of units in the processor core, wherein the units comprise dynamic logic.

19. (Original) The method of claim 8, wherein pre-decoding comprises incorporating a bit in a power token associated with the instructions to maintain inputs for units in the processor core, wherein the units comprise static logic.

20. (Original) The method of claim 8, wherein pre-decoding comprises modifying the frequency and voltage associated with the processor core based upon the dynamic power count.

21. (Original) A method, comprising:

encoding instructions with a power token between levels of cache for a processor core, to monitor power dissipation in the processor core;

determining a dynamic weighted execution rate based upon the power tokens that are associated with instructions executed by the processor core; and

adjusting power dissipation by the processor core based upon the dynamic weighted execution rate.

22. (Original) The method of claim 21, wherein encoding comprises selecting a power token for the instructions from a table of power tokens, wherein the table comprises a pre-determined power token for each of the instructions.

23. (Original) The method of claim 21, wherein determining the dynamic weighted execution rate comprises summing the power tokens upon execution of the instructions and adding the sum to the dynamic weighted execution rate.

24. (Original) The method of claim 21, wherein adjusting the power dissipation comprises modifying execution flags to adjust an issue rate associated with the instructions.

25. (Original) The method of claim 21, wherein adjusting the power dissipation comprises adjusting the frequency and voltage of the processor core.

26. (Original) The method of claim 21, wherein adjusting the power dissipation comprises adjusting a number of the instructions associated with a group to execute in parallel via the processor core.

27. (Original) The method of claim 21, wherein adjusting the power dissipation comprises transmitting a signal to an operating system to switch tasks associated with the processor core.

28. (Cancelled) A method for encoding opcodes of instructions, the method comprising:

ranking the instructions in accordance with a criteria; and

assigning opcodes to the instructions based upon the ranking, wherein each opcode identifies an instruction of the instructions and indicates a relative ranking of the instruction according to the criteria, with respect to the instructions.

29. (Cancelled) The method of claim 28, wherein the opcodes comprise weighted values associated with the criteria.

30. (Cancelled) The method of claim 29, wherein each of the weighted values represents an average power dissipation for an associated instruction of the instructions.

31. (Original) A pre-decoder residing between levels of cache for managing power dissipation in a processor core, the pre-decoder comprising:

a re-encoder to re-encode an opcode of an instruction to incorporate a power token, the power token comprising a bit to indicate a unit of the processor core to turn off during execution of the instruction; and

transform control logic to adjust the power dissipation in the processor core based upon management control bits associated with the power dissipation, in response to a dynamic power count for the processor core.

32. (Original) The pre-decoder of claim 31, further comprising a frequency index coupled with the transform control logic to control the frequency of the processor core and a voltage index coupled with the transform control logic to control the voltage of the processor core.

33. (Original) The pre-decoder of claim 31, further comprising a threshold buffer having a representation of a physical limitation of the processor core, the physical limitation being related to the dynamic power count, wherein the threshold buffer is coupled with the transform control logic to adjust the power dissipation in the processor core.

34. (Original) The pre-decoder of claim 31, further comprising an execution flag register coupled with the transform control logic to modify execution flags associated with the instruction, the execution flags to schedule issuance of the instruction with respect to other instructions in a parallel execution group associated with the instruction.

35. (Original) The pre-decoder of claim 31, wherein the re-encoder comprises a power token table, the power token table having the power token and power tokens for other instructions to be executed by the processor core.

36. (Original) The pre-decoder of claim 31, wherein the re-encoder is configured to select a new opcode that identifies the instruction and power dissipation associated with the instruction.

37. (Original) The pre-decoder of claim 36, wherein the opcode and the new opcode utilize an equal number of bits.

38. (Cancelled) A pre-decoder residing between levels of cache for re-encoding opcodes of instructions, the pre-decoder comprising:

a table having new opcodes for the instructions, wherein each opcode is associated with one of the instructions and indicates a relative ranking of the instructions according to a criteria; and

a re-encoder to match an instruction with a new opcode of the new opcodes in the table based upon an association between the new opcode and the instruction, to replace an opcode of the instruction with the new opcode in response to receiving the instruction.

39. (Cancelled) The pre-decoder of claim 38, wherein the opcodes comprise weighted values associated with the criteria.

40. (Cancelled) The pre-decoder of claim 39, wherein each of the weighted values represents an average power dissipation for an associated instruction of the instructions.

41. (Original) A system, comprising:

a summer to sum power tokens associated with instructions executed by a processor core;

an adder coupled with the summer to generate a dynamic weighted execution rate representative of power dissipation in the processor core based upon the sum;

a register to maintain a dynamic power count based upon the dynamic execution rate; and

a pre-decoder coupled with the register, residing between main memory and a level one cache for the processor core, to associate the power tokens with the instructions and to dynamically adjust power dissipation by the processor core based upon the dynamic power count and a state of management control bits.

42. (Original) The system of claim 41, wherein the pre-decoder comprises a re-encoder to incorporate the power tokens into opcodes associated with the instructions, wherein each power token indicates a relative average power that the associated instruction of the instructions is to consume during execution by the processor core.

43. (Original) The system of claim 42, wherein the power tokens comprise bits to control clock degating of units in the processor core, wherein the units comprise dynamic logic.

44. (Original) The system of claim 42, wherein the power tokens comprise bits to prevent inputs for units in the processor core from changing, wherein the units comprise static logic.

45. (Original) The system of claim 41, wherein the pre-decoder comprises a base pre-decoder to identify a set of the instructions, each instruction of the set having a result that is independent of the results of other instructions in the set.

46. (Original) The system of claim 41, wherein pre-decoding comprises a base pre-decoder to delineate a group of the instructions for parallel execution based upon stop bit execution flags associated with the instructions.

47. (Original) The system of claim 46, wherein pre-decoding comprises a base pre-decoder to select instructions from the group to modify the dynamic power count, based upon the state of management control bits, to determine a parallel instruction issue schedule.

48. (Original) The system of claim 46, wherein the base pre-decoder is configured to adjust the execution flags to decrease the dynamic power count.

49. (Original) The system of claim 41, wherein the pre-decoder is configured to modify a frequency and voltage associated with the processor core.